REMARKS/ARUGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-20 are presently active in this case, Claims 1-8 and 10-19 having been amended and Claim 20 added by the present Amendment.

In the outstanding Office Action, Claim 19 was objected to as including informalities requiring correction. Claims 8, 11, and 18 were rejected under 35 USC §112, first paragraph, as failing to comply with the enablement requirement. Claims 3 and 4 were rejected under 35 USC §112, second paragraph as being indefinite. Claim 1 was rejected under 35 USC §102(a) as being anticipated by Nishigami (5,890,010). Claims 4, 9, 11, 14 and 19 were rejected under 35 USC §103(a) as being unpatentable over Nishigami. Claims 2, 10 and 12 were rejected under 35 USC §103(a) as being unpatentable over Nishigami in view of Laborie (6,003,124). Claims 3 and 13 were rejected under 35 USC §103(a) as being unpatentable over Nishigami in view of Nguyen et al (5,961,628). Claims 5, 6, 7, 8, 15, 16, 17 and 18 were rejected under 35 USC §103(a) as being unpatentable over Nishigami in view of Williams (5,774,704).

In response to the objection to Claim 19, Claim 19 has been amended as suggested in the Official Action. Accordingly, the objection to Claim 19 has been overcome.

Applicants respectfully traverse the rejection Claims 8, 11 and 18 under 35 USC §112, 1st paragraph, because enabling support for the subject matter of Claims 8 and 18 is provided by the disclosure of the circuit 204 in Fig. 3, as described in the specification at page 17, lines 16 – 33, and enabling support for the subject matter of Claim 11 is provided by

the disclosure of the circuit 202, 203, 205 and 206 in Fig.3, as described in the specification at page 15, line 34 to page 16, line 4. In view of the cited support, withdrawal of the rejection of Claims 8, 11 and 18 under 35 USC §112, 1st paragraph, is believed to be in order and is respectfully requested.

In response to the rejection of Claims 3 and 4 under 35 USC §112, 2nd paragraph, Claims 1, 3 and 4 have been amended to provide clear antecedent basis for the "extended instruction" recited in these claims. Accordingly, this ground for rejection is believed to have been overcome.

In light of the several grounds for rejection on the merits, Claims 1, 2, and 12 have been amended to clarify the structure being recited, so that the claimed processor comprises: a processor core for executing an instruction in a pipeline processing; a data memory accessed by said processor core; and an extended arithmetic unit, connected to an exterior of said processor core, for processing an extended instruction decoded in said processor core in the pipeline processing, the extended arithmetic unit executing an arithmetic operation by using arithmetic operation data retained in a register file in said processor core, and outputting a result of an arithmetic operation directly to a memory stage processing in said processor core, and the processor core receiving the result of the arithmetic operation executed by said extended arithmetic unit and inputted therefrom into said register file in said processor core. In addition, the claimed processor core includes a pipeline controller for flushing or stopping the pipeline processing in said extended arithmetic unit. The new features stated in the amended claims finds support at page 11, line 8 to page 15, line 33, and Fig. 3, of Applicants' original disclosure and no new matter has been added.

The claimed configuration enables the pipeline-structured processor core to efficiently utilize the pipeline-structured extended arithmetic unit by using a pipeline control signal, i.e., the extended instruction, to interface between the pipeline-structured processor core and the pipeline-structured extended arithmetic unit, thereby improving system utilization.[1]

In contrast, neither Nishigami nor Laborie discloses or suggests claimed structure or functionality for flushing or stopping the pipeline processing in said extended arithmetic unit. Accordingly, it is respectfully submitted that the outstanding grounds for rejection of Claims 1, 2 and 12 have been overcome by virtue of the clarification added to these claims by the present amendment.

In response to the several grounds for rejection of Claim 10, Claims 10 has been amended and new Claim 20 to clearly patentably define over the cited art. The changes to Claim 10 and new Claim 20 find support in the disclosure as originally filed, including page 20, lines 5 to 27, and Fig. 8, and therefore do not raise a question of new matter.

With regard to newly amended Claim 10 and the common subject matter stated in Claim 20, the claimed extended arithmetic unit includes: a first stage arithmetic circuit; a second stage arithmetic circuit; and a memory access controller configured to control direct access of said data memory by said extended arithmetic unit after an execution of the arithmetic operation by said first stage arithmetic circuit, and to provide the second stage arithmetic circuit with read out data from said data memory as input data for succeeding pipeline processing. This claimed configuration enables the pipeline-structured extended arithmetic unit to directly access and use data stored in the data memory as input data for

[1] See Applicants' specification at page 22, line 13 – page 23, line 4.

subsequent arithmetic operation in the pipeline processing in the pipeline-structured extended arithmetic unit.

In contrast, neither Nishigami nor Laborie discloses or suggests the claimed direct data memory access by the pipeline-structured extended arithmetic unit in order to utilize accessed data from the data memory as input data for subsequent pipeline stage in the extended arithmetic unit. Accordingly, it is respectfully submitted that amended Claim 1 and the claims dependent therefrom, as well as new Claim 20, patentably define over Nishigami, in view of Laborie, Nguyen and Williams.

Consequently, in view of the present amendment and in light of the above comments, the pending claims are believed to be in condition for formal allowance and an early and favorable action to that effect is requested.

Respectfully submitted,

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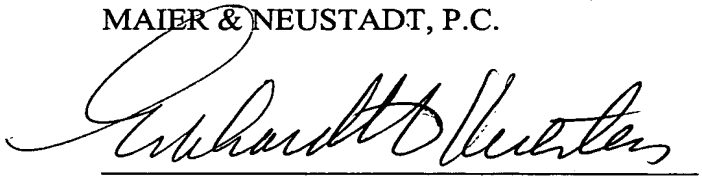

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